41. (Amended) A semiconductor die comprising:

a first planar surface;

a second planar surface opposite the first planar surface;

one or more perimeter edges disposed between the first planar surface and the second planar surface; and

at least one perimeter edge having two or more offset planar [edges] surfaces, where the offset planar [edges] surfaces are substantially transverse to the first planar surface or the second planar surface; and

each offset planar [edge] surface has a flat, smooth surface.

43. (Amended) The semiconductor die as recited in claim 41, wherein the offset planar [edges] surfaces are substantially parallel to one another.

REMARKS

Applicant has carefully reviewed and considered the Office Action mailed on September 25, 2001, and the references cited therewith.

Claims 11, 12, 14 - 18, 20 - 25, 35 - 36, 38 - 41, and 43 are amended; claims 11 - 25 and 35 - 43 remain pending in this application.

Information Disclosure Statement

As requested by the Examiner, Applicant has attached a copy of Form 1449 for the Information Disclosure Statement that was filed with the application on February 16, 2001. Applicant respectfully requests that a copy of the 1449 Form, listing all references that were submitted with the Information Disclosure Statement marked as being considered and initialed by the Examiner, be returned with the next official communication.

Double Patenting Rejection

Claims 11-25 and 35-43 were rejected under the judicially created doctrine of double patenting over claims 1-16 of U.S. Patent No. 6,215,172. Applicant will submit a Terminal Disclaimer upon indication of allowable subject matter.

Claims 11-25 and 35-43 were provisionally rejected under the judicially created doctrine of double patenting over claims 8-10 of copending application No. 09/785,006. Applicant respectfully submits that application no. 09/785,006 is the subject matter of this application, and that claims 8 and 10 were canceled without prejudice in the preliminary amendment dated May 16, 2001. Claim 9 was canceled without prejudice in the preliminary amendment dated February 16, 2001. Withdrawal of the provisional rejection is respectfully solicited.

§112 Rejection of the Claims

Claims 11-25 and 35-43 were rejected under 35 USC § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. The claims were amended to clarify the subject matter therein. The amendments to the claims are fully supported by the specification as originally filed, and no new matter has been added. The amendments are made to clarify the claims and are not intended to limit the scope of equivalents to which any claim element may be entitled. Reconsideration and allowance of claims 11-25 and 35-43 are respectfully requested.

§102 Rejection of the Claims

Claims 11, 13, and 15 were rejected under 35 USC § 102(e) as being anticipated by Mori et al. (U.S. Patent No. 6,287,949) or Badehi (U.S. Patent No. 6,040,235). Applicant respectfully traverses the rejection. Applicant cannot find in Mori or Badehi at least a portion of at least one perimeter side surface of the semiconductor die having a substantially flat, smooth surface as recited in claims 11 and 13. Applicant cannot find in Mori or Badehi one or more perimeter side surfaces extending between the first planar surface and the second planar surface, where at least one perimeter surface has an entirely treated, substantially smooth surface, as recited in claim 15.

Applicant notes that in Badehi, the wafer is diced using a dicing blade. Badehi, Col. 7, Lines 36 - 39. Applicant further notes in Mori, "each of the chip units 32_1 - 32_6 carries a plurality of terminals 33 on the side edges thereof such that the terminals 33 are exposed on the side edges." Mori, Col. 4, Lines 41 - 43. Mori further states "it should be noted that the terminals 33 are formed by providing suitable electrode patterns on a wafer, followed by scribing along the scribe lines. As a result of scribing that divides the wafer into the individual chip unites 32, the

electrode patterns are exposed on the side edges of the chip unites 32 as the terminals 33." Mori, Col. 4, Line 64 - Col. 5, Line 2. It is unclear how either Badehi or Mori provide, among other things, a side surface with a flat, smooth surface as recited in claims 11, 13, and 15.

Reconsideration and allowance of claims 11, 13, and 15 are respectfully requested.

Claims 18-25, 35-37, and 40-43 were rejected under 35 USC § 102(e) as being anticipated by Ishida (U.S. Patent No. 6,117,347). "For a prior art reference to anticipate in terms of 35 U.S.C. § 102, every element of the claimed invention must be identically shown in a single reference." (emphasis added). *In re Bond*, 910 F.2d 831, 15 USPQ2d 1566, 1567 (Fed. Cir. 1990). Applicant respectfully traverses the rejection. Applicant submits that Ishida fails to establish all of the claim elements, and teaches away from the claimed subject matter.

Claims 18 - 21

Applicant respectfully traverses the rejection. Applicant cannot find in Ishida at least one perimeter side surface having at least two offset planar surfaces, where the offset planar surfaces are substantially parallel to each other, and at least one of the two offset planar surfaces of at least one perimeter side surface are substantially flat and smooth, as recited in claims 18 - 21. Furthermore, Applicant cannot find in Ishida, in combination with the elements of claim 18, each perimeter side surface having offset planar surfaces, as recited in claim 20. In addition, Applicant cannot find in Ishida, in combination with the elements of claim 18, each offset planar surface having a substantially smooth and flat surface, as recited in claim 21.

Applicant respectfully traverses the assertion by the Office Action that "[e]ach planar edge is clearly "flat" and "smooth" as seen in the Figures." Page 4, Office Action. Applicant notes in Ishida at Col. 3, Lines 20 - 23 it states "[c]utting section 40 resulting from etching the organic thin-film layers 11 with excimer laser is rough as compared to that resulting from sawing with the blade 30." Unless relying on hindsight reconstruction, the Office Action appears to be taking Official Notice of facts not supported by the Patent. Applicant traverses the Official Notice and respectfully requests a patent under MPEP § 2144.03 to support the assertion, or in the alternative, withdrawal of this assertion from the rejection.

Reconsideration and allowance of claims 18 - 21 are respectfully requested.

Claims 22 - 24

Applicant respectfully traverses the rejection. Applicant incorporates the above discussion of Ishida herein. Furthermore, Applicant cannot find in Ishida means for treating one or more of the perimeter side surfaces of the semiconductor die to provide one or more of the perimeter side surfaces with one or more substantially treated, and smooth surfaces as recited in claim 22. In addition, Applicant cannot find in Ishida, in combination with the elements of claim 22, an entire perimeter side surface having a substantially smooth surface, as recited in claim 23. Furthermore, Applicant cannot find in Ishida, in combination with the elements of claim 22, at least one perimeter side surface having offset planar surfaces, where the offset planar surfaces are each substantially smooth and are substantially parallel to each other, as recited in claim 24.

Reconsideration and allowance are respectfully requested 22 - 24.

Claim 25

Applicant respectfully traverses the rejection. Applicant incorporates the above discussion of Ishida herein. Furthermore, Applicant cannot find in Ishida, among other things, a semiconductor die with each perimeter side surface having offset perimeter planar surfaces, where the perimeter planar surfaces are substantially parallel to each other, and the perimeter planar surfaces are treated, substantially smooth surfaces, as recited in claim 25. Reconsideration and allowance of claim 25 are respectfully requested.

Claims 35 - 37, 40

Applicant respectfully traverses the rejection, and incorporates the above discussion of Ishida herein. Applicant respectfully submits that Ishida teaches away from the claimed subject matter as discussed above, and fails to identically establish all of the elements of the claims. For instance, Applicant cannot find in Ishida, among other things, a semiconductor die having two or more offset planar perimeter surface, where at least one perimeter side surface has a treated, substantially smooth surface, as recited in claims 35 -37, 40. Furthermore, Applicant cannot find in Ishida a semiconductor die where each planar perimeter surface has an entirely flat, smooth surface, as recited in claim 36. Reconsideration and allowance of claims 35 -37, 40 are respectfully requested.

Claims 41 - 43

Applicant respectfully traverses the rejection, and incorporates the above discussion of Ishida herein. Applicant respectfully submits that Ishida teaches away from the claimed subject matter as discussed above, and fails to identically establish all of the elements of the claims. For instance, Applicant cannot find in Ishida, among other things, a semiconductor die having two or more offset planar surface, where each offset planar surface has a treated, substantially smooth surface, as recited in claims 41 - 43. Reconsideration and allowance of claims 41 - 43 are respectfully requested.

Claims 22 and 23 were rejected under 35 USC § 102(e) as being anticipated by Mori et al. (U.S. Patent No. 6,287,949). Applicant respectfully traverses the rejection. "For a prior art reference to anticipate in terms of 35 U.S.C. § 102, every element of the claimed invention must be identically shown in a single reference." (emphasis added). *In re Bond*, 910 F.2d 831, 15 USPQ2d 1566, 1567 (Fed. Cir. 1990). "The identical invention must be shown in as complete detail as is contained in the . . . claim." *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). Applicant cannot find in Mori a semiconductor die that includes a means for treating one or more of the perimeter side surfaces of the semiconductor die to provide one or more of the perimeter side surfaces with one or more substantially flat, treated, and smooth surfaces as recited in claim 22. Furthermore, Applicant cannot find in Mori, in combination with the elements of claim 22, one or more flat, treated, and smooth surfaces, where the entire perimeter side surface is a substantially smooth surface, as recited in claim 23. By failing to teach such structure, Mori does not meet the standard set forth in *In re Bond* requiring that "every element of the claimed invention must be identically shown in a single reference." 910 F.2d at 831, 15 USPQ2d at 1566, 1567.

According to the Office Action, "Mori teaches that the planar edges should be smooth and flat so they can be abutted against other chips [col. 3, lines 6 - 18]." Page 4, Office Action. Applicant respectfully traverses the assertion. Applicant cannot find in the cited text any mention of smooth side surfaces. Unless relying on hindsight reconstruction, the Office Action appears to be taking Official Notice of facts not supported by the Patent. Applicant traverses the Official Notice and respectfully requests a patent under MPEP § 2144.03 to support the assertion,

or in the alternative, withdrawal of this assertion from the rejection.

Applicant notes that in Mori, "the terminals 33 are formed by providing suitable electrode patterns on a wafer, followed by scribing along the scribe lines. As a result of scribing that divides the wafer into the individual chip units 32." Mori, Col. 4, Line 64 - Col. 5, Line 2. Applicant submits that it is unclear how scribing could result in a smooth surface as recited in the claims.

Reconsideration and allowance of claims 22 and 23 is respectfully requested.

§103 Rejection of the Claims

Claims 12 and 17 were rejected under 35 USC § 103(a) as being unpatentable over Mori et al. (U.S. Patent No. 6,287,949) or Badehi (U.S. Patent No. 6,040,235) as applied to claims 11 and 15 above, and further in view Bean et al. (U.S. Patent No. 5,196,378).

Applicant respectfully traverses the rejection. Applicant cannot find in Mori, Badehi, or Bean a semiconductor die with at least a portion of at least one perimeter side surface of the semiconductor die having a substantially flat, smooth surface as recited in claim 11, from which claim 12 depends. Applicant cannot find in Mori or Badehi or Bean, a semiconductor die with one or more perimeter side surfaces extending between the first planar surface and the second planar surface, where at least one perimeter surface has an entirely treated, substantially smooth surface, as recited in claim 15, from which claim 17 depends.

Obviousness is tested by "what the combined teaching of the references would have suggested to those of ordinary skill in the art." *In re Keller*, 642 F.2d 413, 425, 208 USPQ 871, 878 (CCPA 1981)). But it "cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching or suggestion supporting the combination." *ACS Hosp. Sys.*, 732 F.2d at 1577, 221 USPQ at 933. And "teachings of references can be combined only if there is some suggestion or incentive to do so." *Id.* (emphasis in original). The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). A prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention. *W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 USPQ 303

(Fed. Cir. 1983), *cert. denied*, 469 U.S. 851 (1984).

According to the Office Action, "[i]t would have been obvious at the time of applicant's invention to have modified either Mori or Badehi et al. by polishing the edges as was well-known in the art as established by Bean et al. One of ordinary skill in the art would have been motivated to polish the edges to obtain a smooth surface that can be abutted to another chip." Page 5, Office Action.

Applicant respectfully disagrees. Notwithstanding the fact that even if combined, the references fail to establish all of the claims, Applicant respectfully submits that there is no motivation to combine the references. In fact, as the Office Action states, the referenced section in Bean is not a "preferable practice" and therefore teaches away from the claims. One skilled in the art would not be inclined to incorporate a practice that is going to cause damage, and is specifically mentioned as being unpreferable. Furthermore, Mori fails to mention providing a side surface with a smooth, treated surface. It is unclear why one skilled in the art would add extra, damaging steps to achieve the same result, i.e. abutting surfaces. When properly considered as a whole, there is no motivation to combine Bean with Mori and/or Badehi.

Reconsideration and allowance of claims 12 and 17 are respectfully requested.

Claims 25 and 39 were rejected under 35 USC § 103(a) as being unpatentable over Ishida (U.S. Patent No. 6,117,347) as applied to claims 25 and 35 above, and further in view of Bean et al. (U.S. Patent No. 5,196,378). Applicant respectfully traverses the rejection since the references fail to establish all of the elements, and there is no motivation to combine the references. For instance, Applicant cannot find in Ishida or Bean, among other things, a side surface with offset perimeter planar surfaces, where the perimeter surfaces are treated and substantially smooth surfaces as recited in claim 25. Furthermore, Applicant cannot find in Ishida or Bean, among other things, a semiconductor die having two or more offset planar perimieter surfaces, where at least one planar perimeter side surface has a treated, substantially smooth surface, as recited in claim 35, from which claim 39 depends.

Furthermore, obviousness is tested by "what the combined teaching of the references would have suggested to those of ordinary skill in the art." *In re Keller*, 642 F.2d 413, 425, 208 USPQ 871, 878 (CCPA 1981)). But it "cannot be established by combining the teachings of the

prior art to produce the claimed invention, absent some teaching or suggestion supporting the combination." *ACS Hosp. Sys.*, 732 F.2d at 1577, 221 USPQ at 933. And "teachings of references can be combined only if there is some suggestion or incentive to do so." *Id.* (emphasis in original). The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). A prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention. *W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), *cert. denied*, 469 U.S. 851 (1984).

According to the Office Action, "[t]he same arguments apply as in item 9 above, with respect to polishing edges," Paragraph 10, Page 5, Office Action. According to item 9 of the Office Action, "[i]t would have been obvious at the time of applicant's invention to have modified either Mori or Badehi et al. by polishing the edges as was well-known in the art as established by Bean et al. One of ordinary skill in the art would have been motivated to polish the edges to obtain a smooth surface that can be abutted to another chip." Page 5, Office Action.

Applicant respectfully disagrees. Notwithstanding the fact that even if combined, the references fail to establish all of the claims, Applicant respectfully submits that there is no motivation to combine the references. In fact, as the Office Action states, the referenced section in Bean is not a "preferable practice" and therefore teaches away from the claims. One skilled in the art would not be inclined to incorporate a practice that is going to cause damage, and is specifically mentioned as being unpreferable. Furthermore, Ishida fails to mention abutting surfaces of the semiconductor die. With respect to abutting surfaces of a semiconductor die, it is unclear why one skilled in the art would add extra, damaging steps to achieve the same result, i.e. abutting surfaces. The Office Action fails to establish how or why one skilled in the art would be motivated to abut a semiconductor die with offset perimeter planar surfaces with another semicondutor die with offset perimeter planar surfaces. Applicant further notes that Ishida states "[c]utting section 40 resulting from etching the organic thin-film layers 11 with excimer laser is rough as compared to that resulting from sawing with the blade 30." Ishida, Col. 3, Lines 20 - 23. When properly considered as a whole, there is no motivation to combine Bean with Ishida.

Reconsideration and allowance of claims 25 and 39 are respectfully requested.

Claims 14, 16, and 38 were rejected under 35 USC § 103(a) as being unpatentable over Ishida (U.S. Patent No. 6,117,347), Mori et al. (U.S. Patent No. 6,287,949) and/or Badehi (U.S. Patent No. 6,040,235) as applied to claims 11, 15, and 35 above, and further in view of Hart et al. (U.S. Patent No. 5,816,899). Applicant respectfully traverses the rejection, and incorporates herein the above-discussion regarding Ishida, Mori, and Badehi.

To establish a case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the patents themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the patent or to combine patent teachings. Second, there must be a reasonable expectation of success. Finally, the patents must suggest all of the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

"When prior art references require selective combination . . . to render obvious a subsequent invention, there must be some reason for the combination other than the hindsight obtained from the invention itself." *Interconnect Planning Corp. v. Feil*, 774 F.2d 1132, 227 USPQ 543, 551 (Fed. Cir. 1985). "There must be 'something in the prior art as a whole to suggest the desirability, and thus the obviousness, of making the combination'." *Id,* citing *Lindemann Maschinenfabrik GmbH v. American Hoist and Derrick Co.*, 730 F.2d 1452, 1462, 221 USPQ 481, 488 (Fed. Cir. 1984). To be properly considered as prior art in an obviousness determination, a patent must be enabling. *Ashland Oil, Inc. v. Delta Resins and Refractories*, 776 F.2d 281, 297, 227 USPQ 657 (Fed. Cir. 1985), *cert. denied*, 475 U.S. 1017 (1986).

Applicant respectfully traverses the rejection since the cited references fail to establish all of the elements of the claims, and the Office Action fails to provide sufficient motivation to combine the references. For instance, Applicant cannot find in the cited references a semiconductor die with substantially smooth side surfaces, where a layer of scribe material forms the perimeter side surfaces and surrounds the circuitry as recited in claim 11, from which claim 14 depends. Furthermore, Applicant cannot find in the cited references a semiconductor die with at least one perimeter surface having a substantially smooth surface, where a layer of scribe material forms the perimeter side surfaces and surrounds the circuitry as recited in claim 15, from which claim 16 depends. Furthermore, Applicant cannot find in the cited references, in

combination with the elements of claim 15, each entire perimeter side surface having a ground surface as recited in claim 16.

In addition, Applicant cannot find in the cited references a semiconductor die having at least one perimeter side surfaces with two or more offset planar perimeter surfaces with at least one perimeter side surface having a treated, substantially smooth surface, as recited in claim 35, from which claim 38 depends. Applicant notes in Ishida at Col. 3, Lines 20 - 23 it states "[c]utting section 40 resulting from etching the organic thin-film layers 11 with excimer laser is rough as compared to that resulting from sawing with the blade 30." According to Mori, "it should be noted that the terminals 33 are formed by providing suitable electrode patterns on a wafer, followed by scribing along the scribe lines. As a result of scribing that divides the wafer into the individual chip unites 32, the electrode patterns are exposed on the side edges of the chip unites 32 as the terminals 33." Mori, Col. 4, Line 64 - Col. 5, Line 2. Applicant notes that in Badehi, the wafer is diced using a dicing blade. Badehi, Col. 7, Lines 36 - 39. Applicant submits there is no motivation to combine Ishida, Mori and/or Badehi with Hart. Furthermore, even if combined, Applicant respectfully submits the references fail to suggest all of the claim limitations, and it is unclear how the combination would result in the semiconductor die as recited in claim 38.

Reconsideration and allowance of claims 14, 16, and 38 are respectfully requested.

Reservation of Right to Swear Behind References

Applicant reserves the right to swear behind any references which are cited in a rejection under 35 U.S.C. §§102(a), 102(e), 103/102(a), and 103/102(e). Statements distinguishing the claimed subject matter over the cited references are not to be interpreted as admissions that the references are prior art.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 359-3276 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

AARON M. SCHOENFELD

By their Representatives,

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Date 12/26/2001 By _____
Catherine I. Klima-Silberg
Reg. No. 40,052

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 26th day of December, 2001.

Tina Pugh
Name

_____
Signature

OIPE JC42
JAN 25 2002
PATENT & TRADEMARK OFFICE

Docket No. 303.259US3 Micron Ref. No. 96-0587.02
WD # 402391

CLEAN VERSION OF PENDING CLAIMS

GRINDING TECHNIQUE FOR INTEGRATED CIRCUITS
Applicant: Aaron M. Schoenfeld
Serial No.: 09/785,006

Claims 11-25 and 35-43, as of December 26, 2001 (Date of Response to First Office Action).

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11. (Amended) A semiconductor die comprising:

a first planar surface having circuitry thereon;

a second planar surface opposite the first planar surface;

one or more perimeter side surfaces extending between the first planar surface and the second planar surface;

a layer of scribe material forming the perimeter side surfaces, the layer of scribe material surrounding the circuitry; and

at least a portion of at least one perimeter side surface of the semiconductor die having a substantially flat, smooth surface.

12. (Amended) The semiconductor die as recited in claim 11, wherein each perimeter surface has an entirely flat, smooth surface.

13. The semiconductor die as recited in claim 11, wherein the semiconductor die has a substantially rectangular shape.

14. (Amended) The semiconductor die as recited in claim 11, wherein the perimeter surface has a ground surface.

15. (Amended) A semiconductor die comprising:

a first planar surface having circuitry thereon;

a second planar surface opposite the first planar surface;

one or more perimeter side surfaces extending between the first planar surface and the second planar surface; and

at least one perimeter surface having a treated surface, the entire at least one perimeter side surface having a substantially smooth surface;

a layer of scribe material forming the perimeter side surfaces, the layer of scribe material surrounding the circuitry; and

the first planar surface and the second planar surface of the semiconductor die have an overall rectangular shape.

16. (Amended) The semiconductor die as recited in claim 15, wherein each entire side surface comprises a ground surface.

17. (Amended) The semiconductor die as recited in claim 15, wherein the entire side surface comprises a polished surface.

18. (Amended) A semiconductor die comprising:

a first planar surface having circuitry thereon;

a second planar surface opposite the first planar surface;

one or more perimeter side surfaces extending between the first planar surface and the second planar surface; and

at least one perimeter side surface having at least two offset planar surfaces, where the offset planar surfaces are substantially parallel to each other, where at least one of the two offset planar surfaces of at least one perimeter side surface are substantially flat and smooth.

~~19. The semiconductor die as recited in claim 18,~~ wherein the semiconductor die comprises a rectangular die.

20. (Amended) The semiconductor die as recited in claim 18, wherein each perimeter side surface has offset planar surfaces.

21. (Amended) The semiconductor die as recited in claim 18, wherein each offset planar surfaces is substantially smooth and flat.

22. (Amended) A semiconductor die comprising:

a first planar surface having circuitry thereon;

a second planar surface opposite the first planar surface;

one or more perimeter side surfaces extending between the first planar surface and the second planar surface;

a layer of scribe material forming the perimeter side surfaces, the layer of scribe material surrounding the circuitry; and

means for treating one or more of the perimeter side surfaces of the semiconductor die to provide one or more of the perimeter side surfaces with one or more substantially treated, and smooth surfaces.

23. (Amended) The semiconductor die as recited in claim 22, wherein the entire perimeter side surface is a substantially smooth surface.

24. (Amended) The semiconductor die as recited in claim 22, wherein the at least one perimeter side surface has offset planar surfaces, where the planar surfaces are each substantially smooth and are substantially parallel to each other.

25. (Amended) A semiconductor die comprising:

a first planar surface having circuitry thereon;

a second planar surface opposite the first planar surface;

one or more perimeter side surfaces extending between the first planar surface and the

second planar surface;

each perimeter side surface having offset perimeter planar surfaces, where the perimeter planar surfaces are substantially parallel to each other, and the perimeter planar surfaces are treated, substantially smooth surfaces;

a layer of scribe material forming the perimeter side surfaces, the layer of scribe material surrounding the circuitry; and

the semiconductor die has an overall rectangular footprint.

35. (Amended) A semiconductor die comprising:

a first planar surface having circuitry thereon;

a second planar surface opposite the first planar surface;

one or more perimeter side surfaces extending between the first planar surface and the second planar surface; and

at least one perimeter side surface having two or more offset planar perimeter surfaces, at least one perimeter side surface having a treated, substantially smooth surface, where the planar perimeter surfaces are substantially transverse to the first planar surface and the second planar surface.

36. (Amended) The semiconductor die as recited in claim 35, wherein each planar perimeter surface has an entirely flat, smooth surface.

37. The semiconductor die as recited in claim 35, wherein the semiconductor die has a substantially rectangular shape.

38. (Amended) The semiconductor die as recited in claim 35, wherein the planar perimeter surfaces have ground surfaces.

39. (Amended) The semiconductor die as recited in claim 35, wherein the planar perimeter surfaces have polished surfaces.

40. (Amended) The semiconductor die as recited in claim 35, wherein the planar perimeter surfaces are substantially parallel to one another.

41. (Amended) A semiconductor die comprising:

a first planar surface;

a second planar surface opposite the first planar surface;

one or more perimeter edges disposed between the first planar surface and the second planar surface; and

at least one perimeter edge having two or more offset planar surfaces, where the offset planar surfaces are substantially transverse to the first planar surface or the second planar surface; and

each offset planar surface has a flat, smooth surface.

42. The semiconductor die as recited in claim 41, wherein the semiconductor die comprises a rectangular die.

43. (Amended) The semiconductor die as recited in claim 41, wherein the offset planar surfaces are substantially parallel to one another.